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10/085,433	02/28/2002	Yves L. Baeyens	Baeyens 1-24-4-1-1	3191
46850	7590 02/24/2005		EXAMINER	
STEVE ME	ENDELSOHN	LE, TRAN Q		
MENDELSO	OHN & ASSOCIATES, I			
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SUITE 715			2633	
PHILADELPHIA, PA 19102			DATE MAILED: 02/24/200	5

Please find below and/or attached an Office communication concerning this application or proceeding.

		al	
	Application No.	Applicant(s)	
	10/085,433	BAEYENS	
Office Action Summary	Examiner	Art Unit	
	Tran Q. Le	2633	
The MAILING DATE of this communication app Period for Reply	pears on the cover sheet w	ith the correspondence address	•
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a y within the statutory minimum of thi vill apply and will expire SIX (6) MOI, , cause the application to become A	reply be timely filed ty (30) days will be considered timely. NTHS from the mailing date of this communicat BANDONED (35 U.S.C. § 133).	tion.
Status			
1) Responsive to communication(s) filed on 28 Fe	ebruary 2002.		
2a) ☐ This action is FINAL . 2b) ☑ This	action is non-final.		
3) Since this application is in condition for allowar closed in accordance with the practice under E	•	•	is
Disposition of Claims			
 4) Claim(s) 1-20 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) Claim(s) is/are allowed. 6) Claim(s) 1-5,7-20 is/are rejected. 7) Claim(s) 6 is/are objected to. 8) Claim(s) are subject to restriction and/or 	wn from consideration.		
Application Papers			
9) ☐ The specification is objected to by the Examine 10) ☑ The drawing(s) filed on 28 February 2002 is/are Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) ☐ The oath or declaration is objected to by the Ex	e: a) accepted or b) ⊠ drawing(s) be held in abeya tion is required if the drawing	nce. See 37 CFR 1.85(a). I(s) is objected to. See 37 CFR 1.121	
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document: 2. Certified copies of the priority document: 3. Copies of the certified copies of the priority application from the International Bureau. * See the attached detailed Office action for a list	s have been received. s have been received in a rity documents have been u (PCT Rule 17.2(a)).	Application No received in this National Stage	
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	Paper No	Summary (PTO-413) (s)/Mail Date Informal Patent Application (PTO-152) 	

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DETAILED ACTION

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Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation "the amplifier comprises two or more amplification stages" in claim 8 and "the multiplexer includes a phase-locked loop circuit configured to lock the phase of the clock signal to the trunk NRZ data signal" in claim 12 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant

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will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 2-16, 18-20 are objected to because of the following informalities: the preamble "the invention of claim .." is not appropriate and should be changed to "the apparatus according to claim .." or "the method according to claim .." to be consistent with the language of the apparatus/method claimed in the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 7-9,13, 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Givehchi (US Pub. No. 2002/0109893), in view of Adham (US Patent No. 6,100,716).

Regarding claims 1 and 17, Givehchi discloses an apparatus for converting a non-return-to-zero (NRZ) data signal to a return-to-zero (RZ) data signal (abstract and fig. 2), the apparatus comprising: a RZ data signal (output, fig. 3 and p. 2, par. 15) corresponding to the NRZ data signal (data, fig. 3 and p.

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3, par. 18-par. 19) based on (i) the NRZ data signal (data, fig. 3) and (ii) a clock signal (clock, fig. 3) synchronized with the NRZ data signal (fig. 3).

Givehchi differs from the claimed invention in that he does not teach an amplifier configured to generate an amplified RZ data signal, but instead he teaches an electrical data generator for generating a RZ data signal including an AND gate configured to compute an AND function (p. 2, par. 16).

However, Adham, in the same field of endeavor, teaches an AND gate in CML circuits which includes a differential amplifier (fig. 1B and col. 6, lines 48-61).

Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use an AND gate such as the one of Adham in the apparatus of Givehchi in order to provide an RZ data signal with some gain.

Regarding claims 2 and 18, the combination of Givehchi and Adham further teaches the amplifier is a differential amplifier configured to generate the amplified RZ data signal based on a comparison between a first signal corresponding to the NRZ data signal and a second signal corresponding to the clock signal (fig. 2 of Givehchi and fig. 1B of Adham).

Regarding claims 3, 4, and 19, Givehchi in paragraph 0019, lines 14-18 discloses the signal generated 240 and 232 in response to the clock and data signals includes a DC component for achieving linear operation. Therefore, the data and clock signals (first and second signals) must be offset by a DC offset value in order to achieve linear operation.

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Regarding claim 7, the combination of Givehchi and Adham further teaches the differential amplifier comprises a constant current source (22a, fig. 1B of Adham) and two switches connected to the current source (18a, 20a, fig. 1B), wherein the first and second signals (b, bb, fig. 1B) are applied to the two switches to generate the amplified RZ data signal (fig. 1B of Adham).

Regarding claim 8, the combination of Givehchi and Adham further teaches the amplifier comprises two or more amplification stages (fig. 1B of Adham).

Regarding claim 9, the combination of Givehchi and Adham further teaches the apparatus is implemented as an integrated circuit (p. 3, par. 22 of Givehchi and fig. 1B and col. 6, lines 48-61 of Adham).

Regarding claim 13, the combination of Givehchi and Adham further teaches an electro-optic (E/O) modulator (204, fig. 2 of Givehchi) configured to receive an optical input from a laser (230, fig. 2 of Givehchi) and to modulate said optical input using the amplified RZ data signal (236, fig. 2 of Givehchi) to output an optical RZ data signal (output, fig. 2 of Givehchi and p. 2, par. 16) corresponding to the amplified RZ data signal.

Regarding claim 14, the combination of Givehchi and Adham further teaches the laser is configured to generate continuous wave light emission (230, fig. 2 of Givehchi).

4. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Givehchi (US Pub. No. 2002/0109893) in view of Adham (US Patent No. 6,100,716), and in further view of Murai (US Patent No. 6,718,142).

Regarding claim 5, the combination of Givehchi and Adham discloses all the aspects of claims 1 and 2, except fails to teach a circuitry configured to condition at least one of the NRZ data signal and the clock signal to produce at least one of the first and second signals.

However, Murai, in the same field of endeavor, teaches a circuitry (3, fig. 1) configured to condition at least one of the NRZ data signal and the clock signal (optical NRZ signal) to produce at least one of the first and second signals (clock component) (fig. 1 and p. 3, par. 44).

Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to utilize a circuitry such as the one of Murai in the modified device of Givehchi and Adham in order to provide a clock input synchronized with the NRZ data signal by using a simple means/structure.

5. Claims 10, 11, 15, 16, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Givehchi (US Pub. No. 2002/0109893) in view of Adham (US Patent No. 6,100,716) and in further view of the prior art (specification).

Regarding claims 10 and 20, the combination of Givehchi and Adham discloses all the aspects of claim 1, except fails to teach the NRZ data signal is a trunk NRZ data signal; and the apparatus further comprises a multiplexer

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configured to combine two or more tributary NRZ data signals into the trunk NRZ data signal.

However, the prior art discloses the NRZ data signal is a trunk NRZ data signal (NRZ data, fig. 1 and p.1, lines 23-26 of the specification); and the apparatus further comprises a multiplexer (120, fig. 1) configured to combine two or more tributary NRZ data signals (118, fig. 1) into the trunk NRZ data signal (fig. 1 and p.1, lines 23-26 of the specification).

Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to incorporate a multiplexer such as the one of the prior art in the modified apparatus of Givehchi and Adham in order to provide a higher bit rate and capacity for optical data transmission.

Regarding claim 11, the combination of Givehchi, Adham and the prior art further teaches the multiplexer is configured to generate the clock signal (clock, fig. 1 of the prior art and p. 1, lines 23-26 of the specification).

Regarding claim 15, the combination of Givehchi and Adham and the prior art further teaches a multiplexer (120, fig. 1 of the prior art) configured to combine two or more tributary NRZ data signals (118, fig. 1 of the prior art) into the NRZ data signal (NRZ data, fig. 1 of the prior art and specification, p. 1, lines 23-26), wherein: the amplifier is a differential amplifier(fig. 1B of Adham), comprising a constant current source (22a, fig. 1B) and two switches (18a, 20a, fig. 1B) connected to the current source, wherein a first signal corresponding to the NRZ data signal (data, fig. 2 of Givehchi and abstract) and a second signal corresponding to the clock signal (clock, fig. 2 of Givehchi) are applied to said

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two switches to generate the amplified RZ data signal based on a comparison between said first and second signals (fig. 2 of Givehchi and fig. 1B of Adham).

Regarding claim16, the combination of Givehchi and Adham further teaches a laser configured to generate continuous wave light emission (230, fig. 2 of Givehchi); and an electro-optic (E/O) modulator (204, fig. 2 of Givehchi) configured to receive an optical input from the laser and to modulate the optical input using the amplified RZ data signal (217, fig. 2 of Givehchi) to output an optical RZ data signal (Output, fig. 2 of Givehchi) corresponding to the amplified RZ data signal (217, fig. 2 of Givehchi and p. 2, par. 16).

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Givehchi (US Pub. No. 2002/0109893) in view of Adham (US Patent No. 6,100,716) and the prior art (specification), and in further view of Mizoguchi (US Patent No. 6,031,413).

Regarding claim 12, the combination of Givehchi, Adham and the prior art disclose all the aspects of claims 1 and 10, except fails to teach the multiplexer includes a phase-locked loop circuit configured to lock the phase of the clock signal to the trunk NRZ data signal.

However, Mizoguchi, in the same field of endeavor, teaches a multiplexer with a built-in PLL circuit (10, fig. 3 and col. 4, lines 56-60) configured to output a high-speed serial data (88, fig. 3) locked in phase with the input clock (output of TX PLL, fig. 3) based on low-speed parallel data signals (81, fig. 3).

Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to incorporate a multiplexer with a built-in PLL circuit such as the one of Mizoguchi in the modified apparatus of Givehchi, Adham, and the prior art in order to provide a high-speed NRZ data signal synchronized with a clock signal by using a simple configuration from a built-in PLL circuitry to eliminate DC offset induced by nonsymmetrical data.

Allowable Subject Matter

- 7. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 6, the combination of Givehchi, Adham, and Murai still fails to teach specifically the differential amplifier, wherein: (i) if the first signal is greater than the second signal, the amplified RZ data signal is at a low level; and (ii) if the first signal is less than the second signal, the amplified RZ data signal is at a high level.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fukunaga et al. (US Patent No. 5,610,606) is cited to show an RZ signal generating circuit using a 1-bit D/A conversion circuit.

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Kikuchi et al. (US Patent No. 6,850,713) is cited to show a conventional SSB method is applied to an RZ modulated optical transmitter.

Miyamoto et al. (US Patent No. 6,559,996) is cited to show an optical transmission system which reduces optical bandwidth with return-to-zero signal.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tran Q. Le whose telephone number is (571)272-2046. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
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